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JANET FARR
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Date: May 28, 2004

Janet Farr
(Signature of person faxing paper)

Docket No: H0462A **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Applicant: Nian Yang, et al. Examiner: Phuc T. Dang

Serial No.: 10/660,420 Art Unit: 2818

Filing Date: September 10, 2003 Confirmation No. 5813

Title: **HIGH DENSITY FLOATING GATE FLASH MEMORY AND FABRICATION PROCESSES THEREFOR**

REPLY TO OFFICE ACTION MAILED MAY 13, 2004

VIA FACSIMILE
M/S Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Sir:

The present Reply is filed as a complete response to the Office Action mailed May 13, 2004, for which a three month time for reply was set. Accordingly, Applicant's Reply is timely filed. Reconsideration of the application is respectfully requested.

PAGE 1/9 * RCVD AT 5/28/2004 8:54:43 AM [Eastern Daylight Time] * SVR:USPTO-EFXRF-1/3 * DNIS:8729306 * CSID:216 621 6165 * DURATION (mm-ss):02-52

AMENDMENT

Please amend the paragraph at page 1, lines 6-8, to read as follows:

The present application is a division of and claims priority under 35 U.S.C. §120 to copending, commonly owned U.S. Application No. 10/244,229, filed September 16, 2000, now U.S. Patent No. [[_____]] 6,660,588, issued December 09, 2003.

Please amend the paragraph at page 7, lines 25-27, to read as follows:

Fig. 2 illustrates, in cross-section, a floating gate flash memory device in accordance with one embodiment of the present invention, including a floating gate and barrier layer, and a revers reverse tunnel dielectric layer, taken along the bitline direction at line 2-2 of Fig. 20.

In the paragraph on page 17, lines 10-29, please reformat to move the final three sentences into a separate paragraph (no text amendment), appearing as follows:

Referring next to Fig. 6, in the fifth step of the present invention, shown in Fig. 13 as step 1305, an initial trench 44 is formed through the hard mask 40 and pad dielectric 20 layers. In some embodiment, described in more detail below with respect to the processes of Figs. 14, 15, 17 and 18, the initial trench is etched only through the hard mask 40, stopping at the pad oxide layer 20. The initial trench 44 may be formed by any suitable process known in the art. In one embodiment, the etching is an anisotropic, directional etching, e.g., a reactive ion etching. In one embodiment, the etching is an anisotropic dry etch. Appropriate etching methods, including both etchants and etching apparatus, can be selected by those of skill in the art as appropriate. Depending on the particular etching method used, the initial trench 44 is formed typically to include vertical sidewalls 44a, 44b, such as shown in Fig. 6. In one embodiment, not shown, the initial trench may be formed to include non-vertical sidewalls, which would leave structures similar to the sidewall/spacer 36 shown in Fig. 6. However, since purposely forming such non-vertical sidewalls may include additional processing steps, it is generally not done. As shown in Fig. 6, the initial trench 44 has an initial lateral extent, L_i, defined by the opposite hard mask and dielectric layer sidewalls 44a, 44b formed in the hard mask layer 40 and in the dielectric layer 20 by the etching process, as shown in Fig. 6.

In one embodiment, the etchant used to etch the trench 44 comprises a fluoride compound such as CF_4, CHF_3, CH_2F_2 or NF_3. The etchant may further comprise Ar or He. In one embodiment, an Applied Materials 5000 reactor may be used to perform this etch.